

Parametric Filters Laboratory with Noise Generator and Data Acquisition

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Abstract—Audio filtering systems are used in commercial applications involving equalizers. However, some of the topologies used can be modified to be used in audio signal treatment applications. Parametric filter topologies allow the user to modify independently the central frequency of the filter, the bandwidth and the gain. Using a microprocessor and programmable components will allow the user to modify the parameters of the filter and to acquire the filtered signal so it can be processed in other stages. To improve the functionality of the system, a server will be implemented to process the data sent by the user, will be sent afterwards to the microcontroller. Finally, the results obtained will be thrown back to the user.

I. INTRODUCTION

A filter is a circuit which performs signal processing functions, like noise-reduction or enhancing specific frequencies. In this way, a parametric filter is an analog circuit able to modify a signal according to some parameters, which are central Frequency, Gain and Bandwidth. Mostly used in equalization, this kind of filters are worth to implement when it is desired to enhance or suppress a given frequency.

To develop the project (see Fig. 1), four band-pass parametric filters have been implemented. Three of them act as a main modifier of the input signal, and the last one works with the microprocessor as a data acquisition system. These filters have been modified to allow the microprocessor change their parameters.

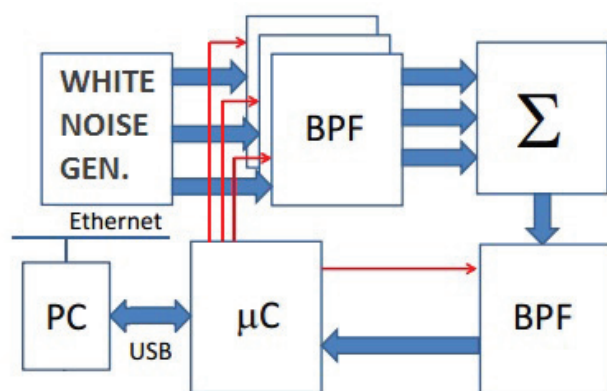


Figure 1. Basic block diagram of the project developed.

The data acquired by the microprocessor will be sent to the computer, to upload them into a server previously created. This server will adapt the data transferred to give the user some bode curves, which will show more accurately the modification of the input signal.

The rest of the paper is organized as follows. Section II provides some information about the structure of the filters and the basic equations. Section III all the considerations taken into account in the final design of the filter. The simulations of the filter behavior are shown in the Section IV. In Section V is provided some explanations about the connections of the filters to the microprocessor, and the data acquisition system. Finally, Section VI shows the main clues about the data transference between the microprocessor and the server. Finally, some concluding remarks are drawn in the last section.

II. FILTER STRUCTURE AND EQUATIONS

The main topology used to implement the filter is the bi-quadratic filter topology [1], [3], [4]. This topology is built around two integrators with two feedback loops that control the central frequency and the bandwidth. This topology has 3 outputs that provide a low-pass filter, a band-pass filter and a high-pass filter. Finally, the gain potentiometer feedbacks the difference between the input and the output into the entry of the bi-quadratic filter (see Fig. 2).

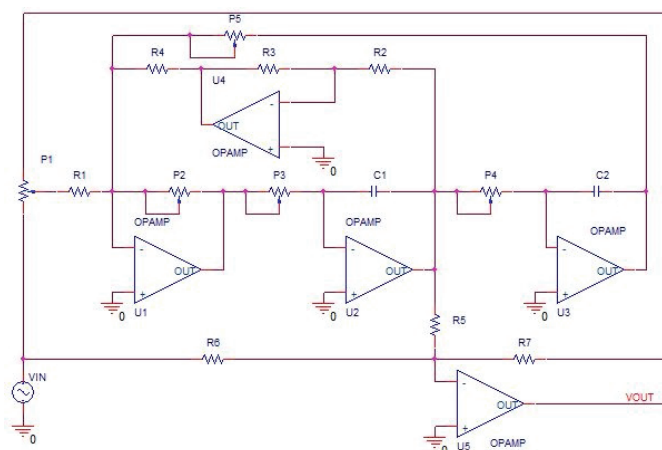


Figure 2. Schematic of the filter in Pspice® OrCAD®.

The bi-quadratic filter equation [2] given the values of the resistances used is shown in (1). To simplify the expression it has been used the following considerations:

- The following resistances take the same value. $R_1=R_2=R_3=R_4=R_6=R_7=R_A$.
- The capacitors take the same value. $C_1 = C_2 = C$.
- The following potentiometers take the same value. $P_3 = P_4 = P_A$.
- The following potentiometers take the same value. $P_2 = P_5 = P_B$.

$$H(s) = \frac{\frac{s}{Q \cdot \omega}}{\frac{s^2}{\omega^2} + \frac{s}{Q \cdot \omega} + 1} = \frac{\frac{P_A \cdot P_B \cdot C \cdot s}{R_A}}{P_A^2 \cdot C^2 \cdot s^2 + \frac{P_A \cdot P_B \cdot C \cdot s}{R_A} + 1} \quad (1)$$

From (1) it can be obtained the central frequency and the quality factor. The final transfer function obtained is showed in (2). As it can be seen on (3), (4) and (5) the equations obtained for the gain, the quality factor and the central frequency are independent, therefore they can be modified individually.

$$\frac{V_{out}}{V_{in}} = \frac{P_1 (x \cdot x^2) + R_A + H(s) \cdot x \cdot \frac{R_A^2}{R_B}}{P_1 (x \cdot x^2) + R_A + H(s) \cdot (1-x) \cdot \frac{R_A^2}{R_B}} \quad (2)$$

$$G = \frac{P_1 (x \cdot x^2) + R_A + R_A \cdot \frac{R_A}{R_B} \cdot (1-x)}{P_1 (x \cdot x^2) + R_A + R_A \cdot \frac{R_A}{R_B} \cdot x} \quad (3)$$

$$Q = \frac{R_A}{P_B} \quad (4)$$

$$\omega = \frac{1}{P_A \cdot C} \quad (5)$$

III. CONSIDERATIONS OF THE FILTER

The final filter implemented requires some extra components to achieve a proper performance. If it is pretended to have a frequency sweep between 10 Hz and 100 kHz that becomes impossible to be achieved with a single capacitor using the components chosen. Using a single capacitor also has problems regarding linearity. If it is plotted equation (2) with a fixed capacitor it can be seen that the relation between the frequency and the value of the potentiometer is exponential. In terms of resolution means that for low values of the potentiometer the variation of the frequency between two close values is too high (see Fig. 3).

TABLE I. CAPACITORS SELECTED FOR THE FINAL DESIGN

Capacitor used	Maximum frequency obtained
1.5 μ F	33.36 Hz
470 nF	112.87 Hz
150 nF	353.67 Hz
47 nF	1128.75 Hz
15 nF	3536.77 Hz
4.7 nF	11287.58 Hz
1.5 nF	35367.76 Hz
470 pF	112875.846 Hz

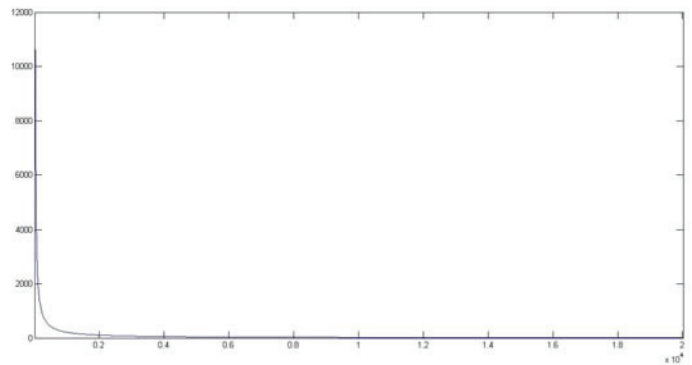


Figure 3. Variation of the frequency for a minimum 10 Hz frequency value for all the possible potentiometer values in MATLAB®.

If it is reduced the range of the potentiometers it can be avoided the increment obtained for the low resistance values of the potentiometer. The final solution to this problem only uses the potentiometer from 20 k Ω to 6 k Ω . In this case (see Fig. 4) the evolution of the frequency is close to being linear.

However, when implementing this solution it is needed to use multiple capacitors to be able to work in the desired frequency spectrum.

The maximum resolution for any given capacitor does not exceed a minimum resolution of 0.3%. This can be problematic at high frequency values because the variation is a percentage. However, given the topology chosen it cannot be changed to a fixed value resolution.

It has been considered to use the capacitor values seen in Table 1. To obtain the desired frequency values two capacitors are put in series to obtain one that halves its initial value and reduces the tolerance of the component. With these capacitors it is almost possible to obtain a linear response through the whole frequency spectrum.

Finally, to implement the design, some specific components must be used.

- To implement the potentiometers, digital potentiometers are be used. It has been chosen the *AD5293* [7] from Analog Devices®. This component offers a very low tolerance and a 10-bit resolution with a value of 20 kΩ.
- To choose different capacitors depending on the desired frequency range, analog multiplexers are used. It has been chosen the *ADG1604* [8] from Analog Devices®. This 4/1 analog multiplexer has a low resistance that minimizes the second order effects.

The implementation of the multiplexers adds a non-desired resistance value to the integrators of the bi-quadratic filter. At high resistance value (see Fig. 5). This additional resistance results on a high frequency constant gain after the central frequency has been reached. However, for low values of the resistance, the high frequency constant gain is too small to be taken in consideration, thus the equations defining the second order effects have not been included.

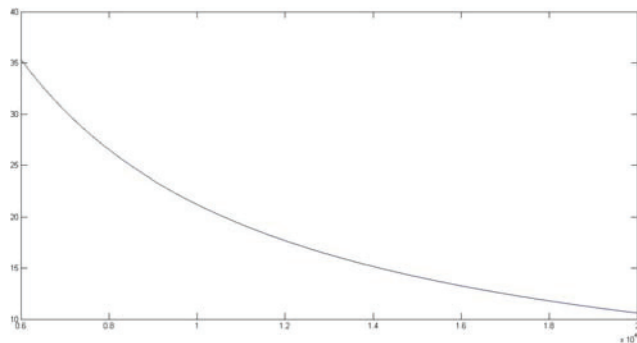


Figure 4. Variation of the frequency for a minimum 10 Hz frequency value for a variation of the potentiometer between 20 kΩ and 6 kΩ in *MatLab*®.

IV. BEHAVIORAL SIMULATIONS

After obtaining all the equations for both cases of the filter described in the Section III, to assure the functionality of the

filter implemented, some simulations have been done.

First of all, this consideration has been taken into account. The first type of simulations stands for the filter with no multiplexers, and the second with them, which include a first order pole into the integrators of the band-pass filter equation. Secondly, it has been considered a variation of the bandwidth, to give acknowledgement about this parameter and how it affects the filter. A variation of the main gain of the filter has been done, to show how it modifies the behavior of the response.

Numerical solutions of the models described in Section III had been obtained by using *Matlab*®, with the compilation of a code created to obtain them. The system is simulated through the whole desired frequency spectrum, from 10 Hz to 100 kHz. The following dynamic behaviors are observed in terms of the parameters chosen.

- $Q = 1.4$: In this case, the system presents a wide bandwidth. Due to this, the gain of the circuit is applied to a large frequency range.
- $Q = 5.0$: For this value of the bandwidth, the system response is narrow than in the other case. This makes the filter more selective through the frequency spectrum.

Apart from the previous considerations to simulate the behavior of the filter, another one has been taken into account. The addition of a multiplexer to obtain the desired frequency spectrum adds a first order pole due to the switching resistance of the multiplexor, as it is said before. For this reason, this pole has been quantified with simulations, with a value of resistance equal to ten, to see how it affects the response of the filter.

Finally, four simulations have been done to acquire all the necessary information to quantify the correct behavior of the system. Each row gives the comparison from the system without multiplexing to the other one, and the difference of the

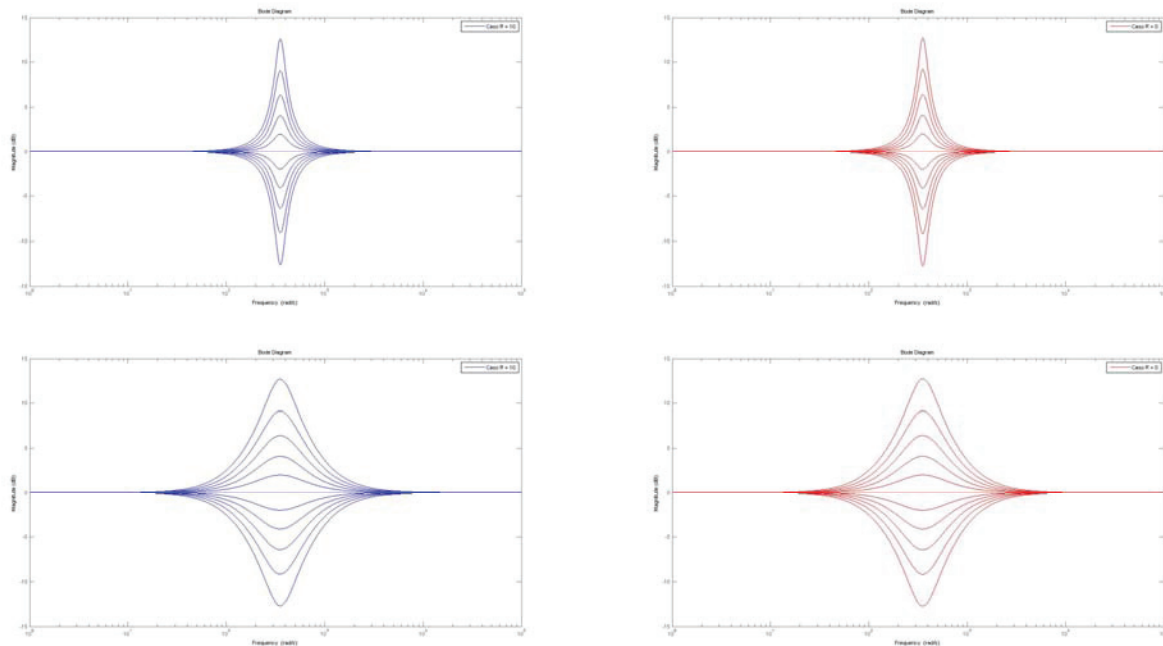


Figure 5. Responses of the filter for different behaviors corresponding to the different values of the control parameters. The first column shows the filter with multiplexing, the second one the normal filter. Top row: $Q=5.0$, both responses show a huge selectivity through the frequency spectrum. There are no appreciable differences between both responses. Bottom row: $Q=1.4$, both responses show less selectivity than in the first case. There are no differences between responses.

bandwidths. To end with, all of the plots shows a variation of the gain.

V. SYSTEM CONNECTION

In this section are explained the connections between the filters and the microprocessor [5]. Also there are explained the connections through the CPLD [6] implemented, to allow the microprocessor change the state of the potentiometers using less bits.

First of all, it must be taken into account that the filters configuration will be in two modes. The first mode stands for a series configuration, where the output of the first filter is connected to the input of the second one, and all in this way.

The second mode works as a parallel configuration of all three filters. Finally, the output of these modes is connected to the last filter, which works as a pointer, to give information to the microprocessor of the signal in the desired frequency.

To use the pointer, the filter is enabled with a specific value for their potentiometers, which will use a high quality factor value and a particular central frequency. With this, the pointer will give the microprocessor the value in this frequency, in an accurately way due to the high quality factor. This value will be taken by the analog-to-digital converter included in the microprocessor, storing it until it is sent back to the PC.

On the other hand, the CPLD works as a transference enabler to the potentiometers in the circuit. As the implemented filter has twenty potentiometers in its schematic, is needed a way to change their value using the minimum number of bits possible. In this way, a de-multiplexer has been implemented, using five control bits. With this, the potentiometers can be enabled just changing the five bits sequence.

Finally, the multiplexers of the board, used to switch between the capacitors to obtain the quoted frequency range, are connected to the microprocessor, which changes the channel used.

VI. DATA TRANSFER

This section explains how the data obtained by the pointer filter and converted to bits through the analog-to-digital converter of the microprocessor is transferred to the computer. Moreover, there is slightly explained how will work the server connection, which will allow the users to perform their calculus from home with the designed board.

Firstly, the data acquired from the analog-to-digital converter is stacked momentarily into the memory of the microprocessor. Later, this data is send using RS-232 protocol to a RS-232 to USB converter. This is done to avoid using the microprocessor USB host. The converter changes the protocol

of sending data, and sends it through the USB connection to the computer.

Secondly, the data arrives to its destiny. Then, it is processed by the computer, which stacks the values onto a file. This file is loaded to the server, which converts the values of it into a plot. This plot is shown to the user, including the table of values for posterior plots.

Finally, to load the values of the parameters of the filter, the same way as the shown before is done, but in the reverse order. First, the user gives the parameters to the server. The server converts them into a data file, and sends it to the computer. When the file arrives at the computer, it is modified to obtain the required values for each component of the filter, to obtain the parameters set previously by the user. These values are sent to the microprocessor, which distributes them to the different devices of the filter board.

VII. CONCLUSIONS

In this paper is shown an overall summary about the project developed, emphasizing the most important parts of it. Firstly, this paper shows the adaptation of the filter to our design, using the multiplexer system, and giving some clues to do it. In second place, the simulations give the necessary information to verify the correct operation of the system implemented, in comparison to the first filter. In third place, some clues about the data acquisition and transmission in all the circuit are given, like the protocols used or the configuration of the transmissions.

To sum up, is important to highlight that the results obtained in this work can provide some help to acquire a higher frequency range, and some basic level about the data acquisition and transmission.

ACKNOWLEDGMENTS

This work has been partially supported by the Spanish Ministerio de Economía y Competitividad by project DPI2013-47799-C2-2-R.

REFERENCES

- [1] S. Franco, "Diseño con amplificadores operacionales y circuitos integrados analógicos", 3rd ed, Mc Graw Hill, 2002, pp. 150–153.
- [2] K. Ogata, Modern Control Engineering, 3rd ed, Prentice-Hall, 1998, pp. 87–91.
- [3] A. Sedra and K. Smith, Microelectronic Circuits, 4th ed, Oxford University Press, 1998, pp. 938–944.
- [4] G. Clayton and S. Winder, Operational Amplifiers, 5th ed, Newnes-Butterworth, 2003, pp 248–251.
- [5] Microchip Technology Inc, "PIC18F4550 Data Sheet", Revision E, 2009.
- [6] Xilinx Inc, "XC2C64A CoolRunner-II CPLD", Revision 2.31, 2008
- [7] Analog Devices Inc, "AD5293 Data Sheet", Revision D, 2011.
- [8] Analog Devices Inc, "ADG1604 Data Sheet", Revision A, 2009.